

# **Manual of compact model for Negative Capacitance Enhanced**

## **Spintronics Devices**

### ***SPINLIB: Model NC\_VCMA\_MTJ***

#### ***Version: Beta\_1.0***

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## **I. General Introduction**

Although spin transfer torque (STT)-based magnetic tunneling junction (MTJ) owns advantages of nonvolatility, nonlimited endurance, and fast write/read, its demand for high current density significantly casts a shadow over its future prospects. Recently, a novel three-terminal MTJ cell that combines voltage-controlled magnetic anisotropy (VCMA) effect and negative capacitance (NC) effect is proposed. Drawing support from the NC amplified VCMA effect and the three-step operation scenario, this novel MTJ cell can dramatically lower the energy consumption to fJ as well as keep high operation speed within nanoseconds. The feasibility of the proposed NC enhanced

VCMA spintronics device for memory and logic application is proved by extensive physical simulation in our previous work. However, a SPICE compatible compact model of the proposed NC enhanced VCMA spintronics device is still demanded for circuit and system level evaluation. In this paper, we provide an accurate and fast compact model of NC enhanced VCMA device for both memory and logic applications.

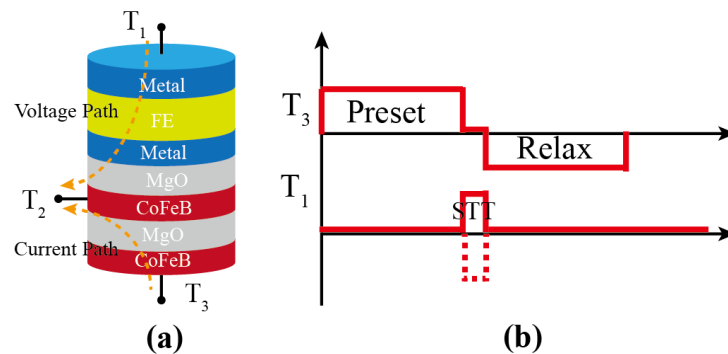


Fig. 1. (a) Illustration of the proposed three-terminal NC enhanced VCMA spintronics devices. (b) Waveforms for the three-step operation scenario. The three stages are the Preset stage, the STT pulse stage, and the Relaxation stage.

**Programmed with Verilog-A language**

**Validated in Cadence 6.1.5 Spectre, CMOS Design Kit 40nm.**

## II. Files Provided and Simulation Results

Decompress the compressed file Model\_NC\_VCMA\_MTJ.zip which you have downloaded (Attention: Never rename the model out of Cadence, or a hierarchical problem would occur.), and six files will appear.

The first file named “NC\_VCMA\_MTJ” includes a script file of the type of verilog, which is the source code of this model, and a symbol file (original symbol). Fig. 2. shows the validation of this compact model without stochastic effect. And Fig. 3. Shows the simulation with stochastic effect.

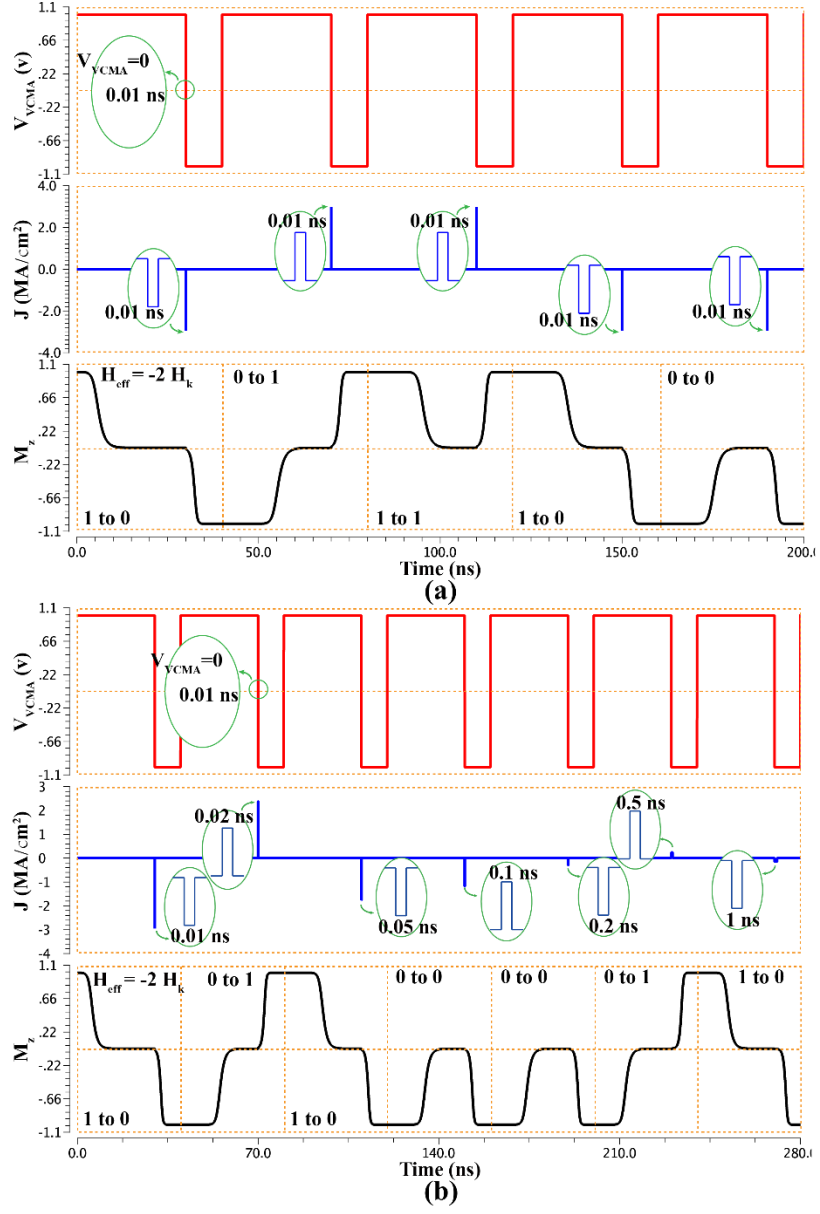


Fig. 2. Validation of the SPICE model without stochastic effect. (a) Simulation with the same combination of current density and duration under  $H_{\text{eff}} = -2 \times H_k$  for four kind of writing conditions. (b) Simulation with different combinations of current density and duration under  $H_{\text{eff}} = -2 \times H_k$ .

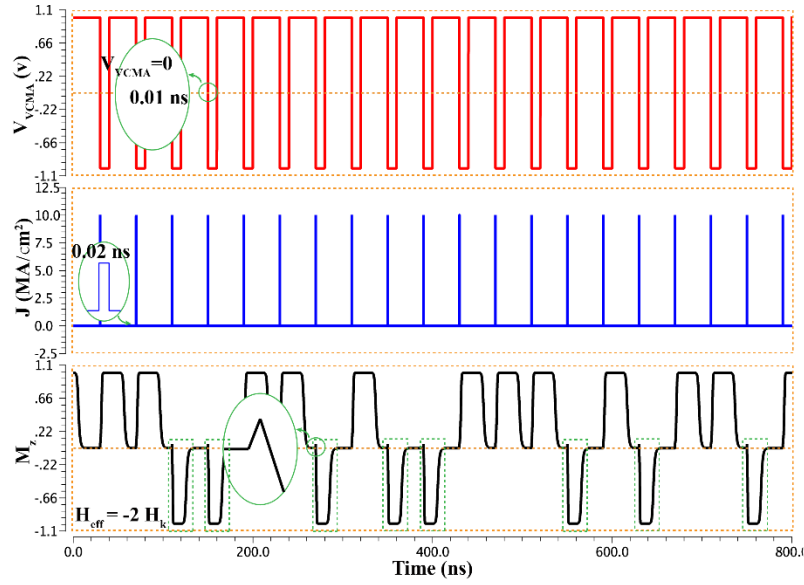


Fig. 3. Simulating the manipulation of writing “1” for 20 times with stochastic effect. Green boxes: wrong switching due to the stochastic effect.

The second file named “Components of NC-VCMA-Devices” includes three files. Injector and detector are designed with the original symbol and a symbol file of NC-VCMA-MTJ (formal symbol). Channel is proposed according to spin-dependent and 1-D drift-diffusion theory. The file “Majority\_Gate” and file “1bit\_fulladder” are designed with the symbol in the file “Components of NC-VCMA-Devices”. Fig. 4. illustrates the simulation results.

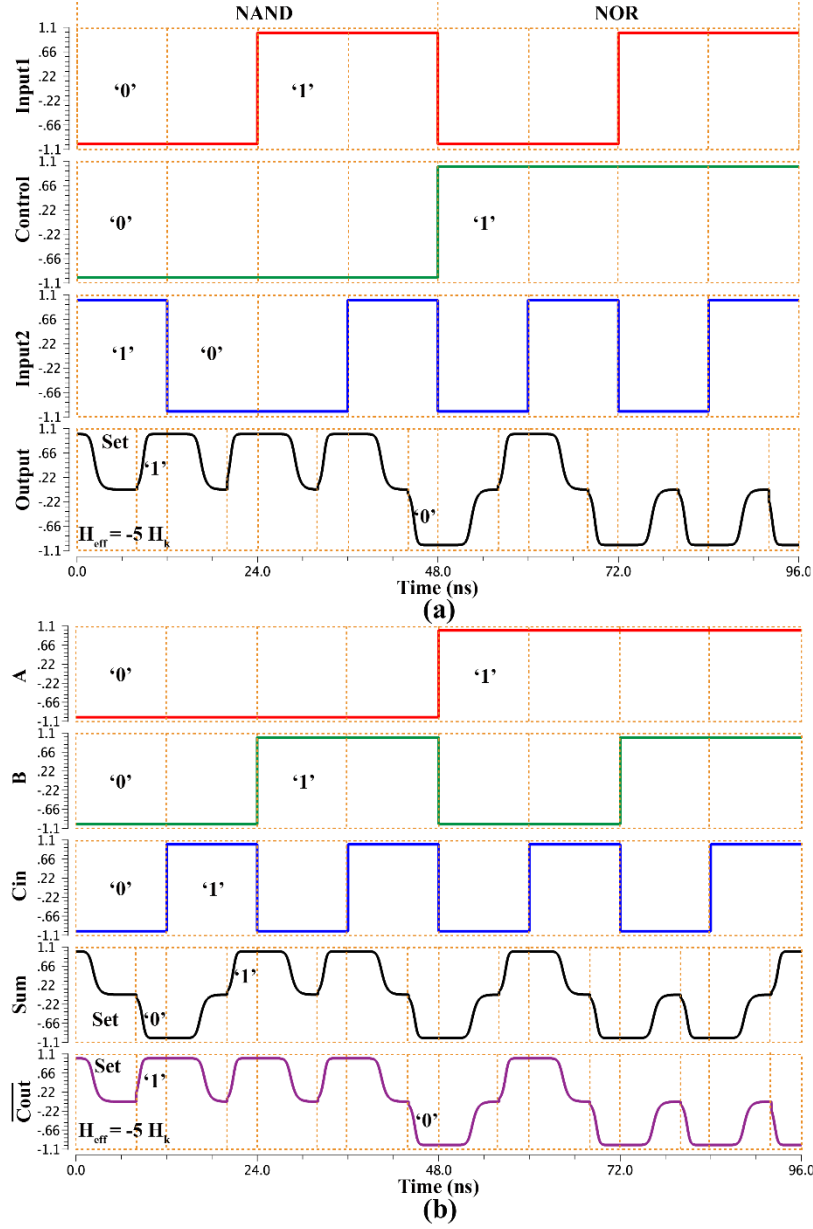


Fig. 4. (a) Simulation results for the case of NAND/NOR logic operations. (b) Simulation results for the 1-bit full adder.

### III. Summary

The dependence of switching time in the Preset stage with the negative effective PMA field is derived analytically. The switching probability of the NC enhanced VCMA devices can be expressed by a linear function of the angle deviated from the in-plane direction caused by the STT pulse current. Based on the compact model of NC enhanced VCMA devices, the SPICE model for both memory and logic application is

provided and validated. Utilizing this SPICE model, circuit design and system evaluation of NC enhanced VCMA devices can be performed and optimized in the future work.

#### IV. References